FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11124-1E

*MEMORY*

**Unbuffered**

# 2 M × 72 BIT SYNCHRONOUS DYNAMIC RAM DIMM

# MB8502S072BZ-75/-102/-10

**168-pin, 4 Clock, 1-bank, based on 2 M × 8 Bit SDRAMs with SPD**



## ■ DESCRIPTION

The Fujitsu MB8502S072BZ is a fully decoded, CMOS Synchronous Dynamic Random Access Memory (SDRAM) Module consisting of nine MB81F16822B devices which organized as two banks of 2 M × 8 bits and a 2K-bit serial EEPROM on a 168-pin glass-epoxy substrate.

The MB8502S072BZ features a fully synchronous operation referenced to a positive edge clock whereby all operations are synchronized at a clock input which enables high performance and simple user interface coexistence.

The MB8502S072BZ is optimized for those applications requiring high speed, high performance and large memory storage, and high density memory organizations.
This module is ideally suited for workstations, PCs, laser printers, and other applications where a simple interface is needed.

## ■ PRODUCT LINE & FEATURES

| Parameter | | MB8502S072BZ-75 | MB8502S072BZ-102 | MB8502S072BZ-10 |
|---|---|---|---|---|
| Clock Frequency | | 133 MHz max. | 100 MHz max. | 100 MHz max. |
| Burst Mode Cycle Time | | 7.5 ns max. | 10 ns max. | 10 ns max. |
| Output Valid from Clock | | 6 ns max.(CL=3) | 6 ns max. (CL = 2) | 6 ns max. (CL = 3) |
| Power Dissipation | Two Banks Active | 4860 mW max. | 4536 mW max. | 3888 mW max. |
| | Self Refresh Mode | 12.96 mW max. | | |

- Unbuffered 168-pin DIMM Socket Type
  (Lead pitch: 1.27 mm)
- Conformed to JEDEC Standard (4 CLK)
- Organization: 2,097,152 words × 72 bits
- Memory: MB81F16822B (2 M × 8, 2-bank) × 9 pcs.
- 3.3 V ±0.3 V Supply Voltage
- All input/output LVTTL compatible
- Conformed to Intel PC/100 spec
- 4096 Refresh Cycle every 65.6 ms
- Auto and Self Refresh
- CKE Power Down Mode
- DQM Byte Masking (Read/Write)
- Serial Presence Detect (SPD) with Serial EEPROM:
  JEDEC Standard SPD Format
- Module size:
  1.35” (height) × 5.25” (length) × 0.157” (thickness)

# MB8502S072BZ-75/-102/-10

## ■ PACKAGE

168-pin plastic DIMM (socket type)

**T.B.D.**

(MDS-168P-P25)

**Package and Ordering Information**

– 168-pin DIMM, order as MB8502S072BZ-××DG (DG = Gold Pad)

# MB8502S072BZ-75/-102/-10

## ■ PIN ASSIGNMENTS

| Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name | Pin No. | Signal Name |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 29 | $DQMB_1$ | 57 | $DQ_{18}$ | 85 | $V_{SS}$ | 113 | $DQMB_5$ | 141 | $DQ_{50}$ |
| 2 | $DQ_0$ | 30 | $\overline{CS}_0$ | 58 | $DQ_{19}$ | 86 | $DQ_{32}$ | 114 | N.C. | 142 | $DQ_{51}$ |
| 3 | $DQ_1$ | 31 | N.C. | 59 | $V_{CC}$ | 87 | $DQ_{33}$ | 115 | $\overline{RAS}$ | 143 | $V_{CC}$ |
| 4 | $DQ_2$ | 32 | $V_{SS}$ | 60 | $DQ_{20}$ | 88 | $DQ_{34}$ | 116 | $V_{SS}$ | 144 | $DQ_{52}$ |
| 5 | $DQ_3$ | 33 | $A_0$ | 61 | N.C. | 89 | $DQ_{35}$ | 117 | $A_1$ | 145 | N.C. |
| 6 | $V_{CC}$ | 34 | $A_2$ | 62 | N.C. | 90 | $V_{CC}$ | 118 | $A_3$ | 146 | N.C. |
| 7 | $DQ_4$ | 35 | $A_4$ | 63 | N.C. | 91 | $DQ_{36}$ | 119 | $A_5$ | 147 | N.C. |
| 8 | $DQ_5$ | 36 | $A_6$ | 64 | $V_{SS}$ | 92 | $DQ_{37}$ | 120 | $A_7$ | 148 | $V_{SS}$ |
| 9 | $DQ_6$ | 37 | $A_8$ | 65 | $DQ_{21}$ | 93 | $DQ_{38}$ | 121 | $A_9$ | 149 | $DQ_{53}$ |
| 10 | $DQ_7$ | 38 | $A_{10}$ | 66 | $DQ_{22}$ | 94 | $DQ_{39}$ | 122 | $BA_0$ | 150 | $DQ_{54}$ |
| 11 | $DQ_8$ | 39 | N.C. | 67 | $DQ_{23}$ | 95 | $DQ_{40}$ | 123 | N.C. | 151 | $DQ_{55}$ |
| 12 | $V_{SS}$ | 40 | $V_{CC}$ | 68 | $V_{SS}$ | 96 | $V_{SS}$ | 124 | $V_{CC}$ | 152 | $V_{SS}$ |
| 13 | $DQ_9$ | 41 | $V_{CC}$ | 69 | $DQ_{24}$ | 97 | $DQ_{41}$ | 125 | $CLK_1$ | 153 | $DQ_{56}$ |
| 14 | $DQ_{10}$ | 42 | $CLK_0$ | 70 | $DQ_{25}$ | 98 | $DQ_{42}$ | 126 | N.C. | 154 | $DQ_{57}$ |
| 15 | $DQ_{11}$ | 43 | $V_{SS}$ | 71 | $DQ_{26}$ | 99 | $DQ_{43}$ | 127 | $V_{SS}$ | 155 | $DQ_{58}$ |
| 16 | $DQ_{12}$ | 44 | N.C. | 72 | $DQ_{27}$ | 100 | $DQ_{44}$ | 128 | $CKE_0$ | 156 | $DQ_{59}$ |
| 17 | $DQ_{13}$ | 45 | $\overline{CS}_2$ | 73 | $V_{CC}$ | 101 | $DQ_{45}$ | 129 | N.C. | 157 | $V_{CC}$ |
| 18 | $V_{CC}$ | 46 | $DQMB_2$ | 74 | $DQ_{28}$ | 102 | $V_{CC}$ | 130 | $DQMB_6$ | 158 | $DQ_{60}$ |
| 19 | $DQ_{14}$ | 47 | $DQMB_3$ | 75 | $DQ_{29}$ | 103 | $DQ_{46}$ | 131 | $DQMB_7$ | 159 | $DQ_{61}$ |
| 20 | $DQ_{15}$ | 48 | N.C. | 76 | $DQ_{30}$ | 104 | $DQ_{47}$ | 132 | N.C. | 160 | $DQ_{62}$ |
| 21 | $CB_0$ | 49 | $V_{CC}$ | 77 | $DQ_{31}$ | 105 | $CB_4$ | 133 | $V_{CC}$ | 161 | $DQ_{63}$ |
| 22 | $CB_1$ | 50 | N.C. | 78 | $V_{SS}$ | 106 | $CB_5$ | 134 | N.C. | 162 | $V_{SS}$ |
| 23 | $V_{SS}$ | 51 | N.C. | 79 | $CLK_2$ | 107 | $V_{SS}$ | 135 | N.C. | 163 | $CLK_3$ |
| 24 | N.C. | 52 | $CB_2$ | 80 | N.C. | 108 | N.C. | 136 | $CB_6$ | 164 | N.C. |
| 25 | N.C. | 53 | $CB_3$ | 81 | N.C. | 109 | N.C. | 137 | $CB_7$ | 165 | $SA_0$ |
| 26 | $V_{CC}$ | 54 | $V_{SS}$ | 82 | SDA | 110 | $V_{CC}$ | 138 | $V_{SS}$ | 166 | $SA_1$ |
| 27 | $\overline{WE}$ | 55 | $DQ_{16}$ | 83 | SCL | 111 | $\overline{CAS}$ | 139 | $DQ_{48}$ | 167 | $SA_2$ |
| 28 | $DQMB_0$ | 56 | $DQ_{17}$ | 84 | $V_{CC}$ | 112 | $DQMB_4$ | 140 | $DQ_{49}$ | 168 | $V_{CC}$ |

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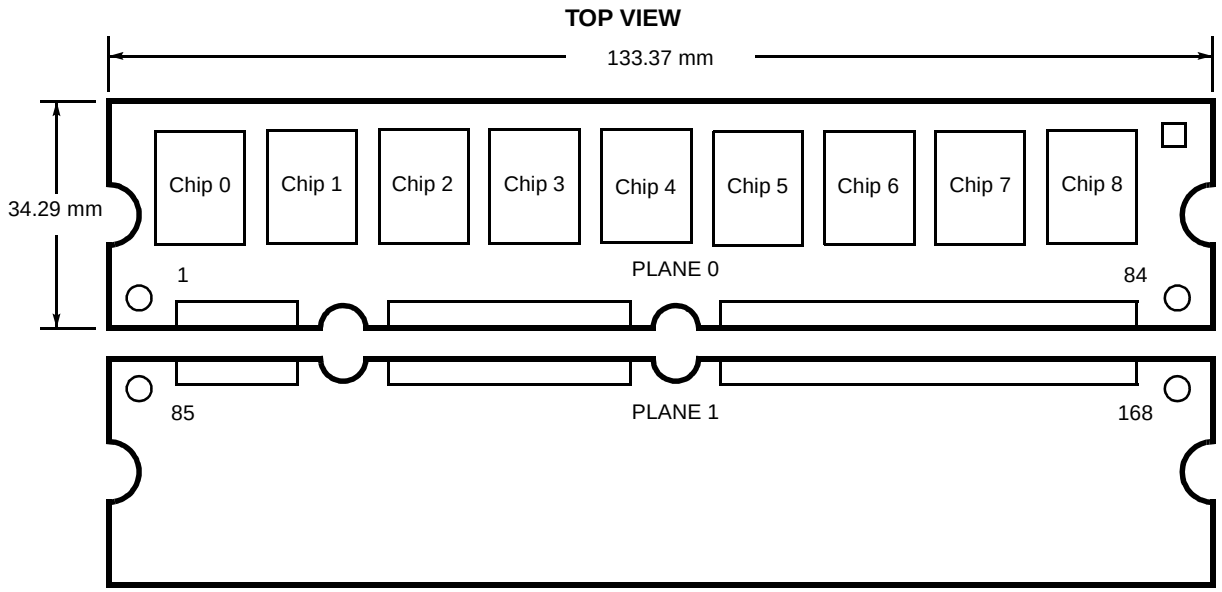


**(MDS-168P-25)**

## ■ PIN DESCRIPTIONS

| Symbol | I/O | Function | Symbol | I/O | Function |
|---|---|---|---|---|---|
| $A_0$ to $A_{10}$, $BA_0$ | I | Address Input | $DQ_0$ to $DQ_{63}$ | I/O | Data Input/Data Output |
| $\overline{RAS}$ | I | Row Address Strobe | $CB_0$ to $CB_7$ | I/O | ECC Data Input/Output |
| $\overline{CAS}$ | I | Column Address Strobe | $V_{CC}$ | — | Power Supply (+3.3 V) |
| $\overline{WE}$ | I | Write Enable | $V_{SS}$ | — | Ground (0 V) |
| $DQMB_0$ to $DQMB_7$ | I | Data (DQ) Mask | N.C. | — | No Connection |
| $CLK_0$ to $CLK_3$ | I | Clock Input | $SA_0$ to $SA_2$ | I | Serial PD Address Input |
| $CKE_0$ | I | Clock Enable | SCL | I | Serial PD Clock |
| $\overline{CS_0}$, $\overline{CS_2}$ | I | Chip Select | SDA | I/O | Serial PD Address/Data Input/Output |

## ■ SERIAL-PD INFORMATION

| Byte | Function Described | | Hex Value | | |
|---|---|---|---|---|---|
| | | | -75 | -102 | -10 |
| 0 | Defines Number of Bytes Written into Serial Memory at Module Manufacture | 128 Byte | 80h | 80h | 80h |
| 1 | Total Number of Bytes of SPD Memory Device | 256 Byte | 08h | 08h | 08h |
| 2 | Fundamental Memory Type | SDRAM | 04h | 04h | 04h |
| 3 | Number of Row Addresses | 11 | 0Bh | 0Bh | 0Bh |
| 4 | Number of Column Addresses | 9 | 09h | 09h | 09h |
| 5 | Number of Module Banks | 1 bank | 01h | 01h | 01h |
| 6 | Data Width | 72 bit | 48h | 48h | 48h |
| 7 | Data Width (Continuation) | +0 | 00h | 00h | 00h |
| 8 | Interface Type | LVTTL | 01h | 01h | 01h |
| 9 | SDRAM Cycle Time (Highest CAS Latency) | 7.5/10/10 ns | 75h | A0h | A0h |
| 10 | SDRAM Access from Clock (Highest CAS Latency) | 6/6/6 ns | 60h | 60h | 60h |
| 11 | DIMM Configuration Type | ECC | 02h | 02h | 02h |
| 12 | Refresh Rate/Type | Self, Normal | 80h | 80h | 80h |
| 13 | Primary SDRAM Width | ×8 | 08h | 08h | 08h |
| 14 | Error Checking SDRAM Width | ×8 | 08h | 08h | 08h |
| 15 | Minimum Clock Delay for Back to Back Random Column Addresses | 1 Cycle | 01h | 01h | 01h |
| 16 | Burst Lengths Supported | 1, 2, 4, 8, Page | 8Fh | 8Fh | 8Fh |
| 17 | Number of Banks on Each SDRAM Device | 2 bank | 02h | 02h | 02h |
| 18 | CAS Latency | 2, 3 | 06h | 06h | 06h |
| 19 | CS Latency | 0 | 01h | 01h | 01h |
| 20 | Write Latency | 0 | 01h | 01h | 01h |
| 21 | SDRAM Module Attributes | UN-buffer | 00h | 00h | 00h |
| 22 | SDRAM Device Attributes | *1 | 06h | 06h | 06h |
| 23 | SDRAM Cycle Time (2nd. Highest CAS Latency) | 11.5/10/15 ns | B5h | A0h | A5h |
| 24 | SDRAM Access from Clock (2nd. Highest CAS Latency) | 7/6/8 ns | 70h | 60h | 80h |
| 25 | SDRAM Cycle Time (3rd. Highest CAS Latency) | No Support | 00h | 00h | 00h |
| 26 | SDRAM Access from Clock (3rd. Highest CAS Latency) | No Support | 00h | 00h | 00h |
| 27 | Minimum Row Precharge Time ($t_{RP}$) | 22.5/20/30 ns | 17h | 14h | 1Eh |
| 28 | Row Activate to Row Activate Min. ($t_{RRD}$) | 15/20/20 ns | 0Fh | 14h | 14h |
| 29 | $\overline{RAS}$ to $\overline{CAS}$ Delay Min. ($t_{RCD}$) | 22.5/20/30 ns | 17h | 14h | 1Eh |
| 30 | Minimum RAS Pulse Width | 45/50/50 ns | 2Dh | 32h | 32h |
| 31 | Module Bank Density | 16 MByte | 04h | 04h | 04h |
| 32 to 61 | Unused Storage Locations | — | 00h | 00h | 00h |
| 62 | SPD Data Revision Code | 1 | 01h | 01h | 01h |
| 63 | Checksum for Byte 0 to 62 | *2 | 85h | 8Fh | C8h |
| 64 to 98 | Manufacturer's Information: Unused Storage | — | 00h | 00h | 00h |
| 99 to 125 | Vendor Specific Data: Unused Storage | — | 00h | 00h | 00h |
| 126 | Intel Specification Frequency | 66 MHz | 66h | 66h | 66h |
| 127 | Intel Specification CAS Latency Support | CL = 2 | 02h | 02h | 02h |
| 128+ | Unused Storage Locations | — | — | — | — |

**Note:** Any write operation must NOT be executed into the addresses of Byte 0 to Byte 127. Some or all data stored into Byte 0 to Byte 127 may be broken.

*1. Byte 22: SDRAM Device Attributes

| Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
|---|---|---|---|---|---|---|---|
| TBD | TBD | Upper $V_{CC}$ tolerance | Lower $V_{CC}$ tolerance | Supports Write 1 /Read Burst | Supports Precharge All | Supports Auto-Precharge | Supports Early $\overline{RAS}$ Precharge |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |

*2. byte 63: Checksum for Bytes 0 to 62
This byte is the checksum for bytes 0 through 62. This byte contains the value of the low 8-bits of the arithmetic sum of bytes 0 through 62.

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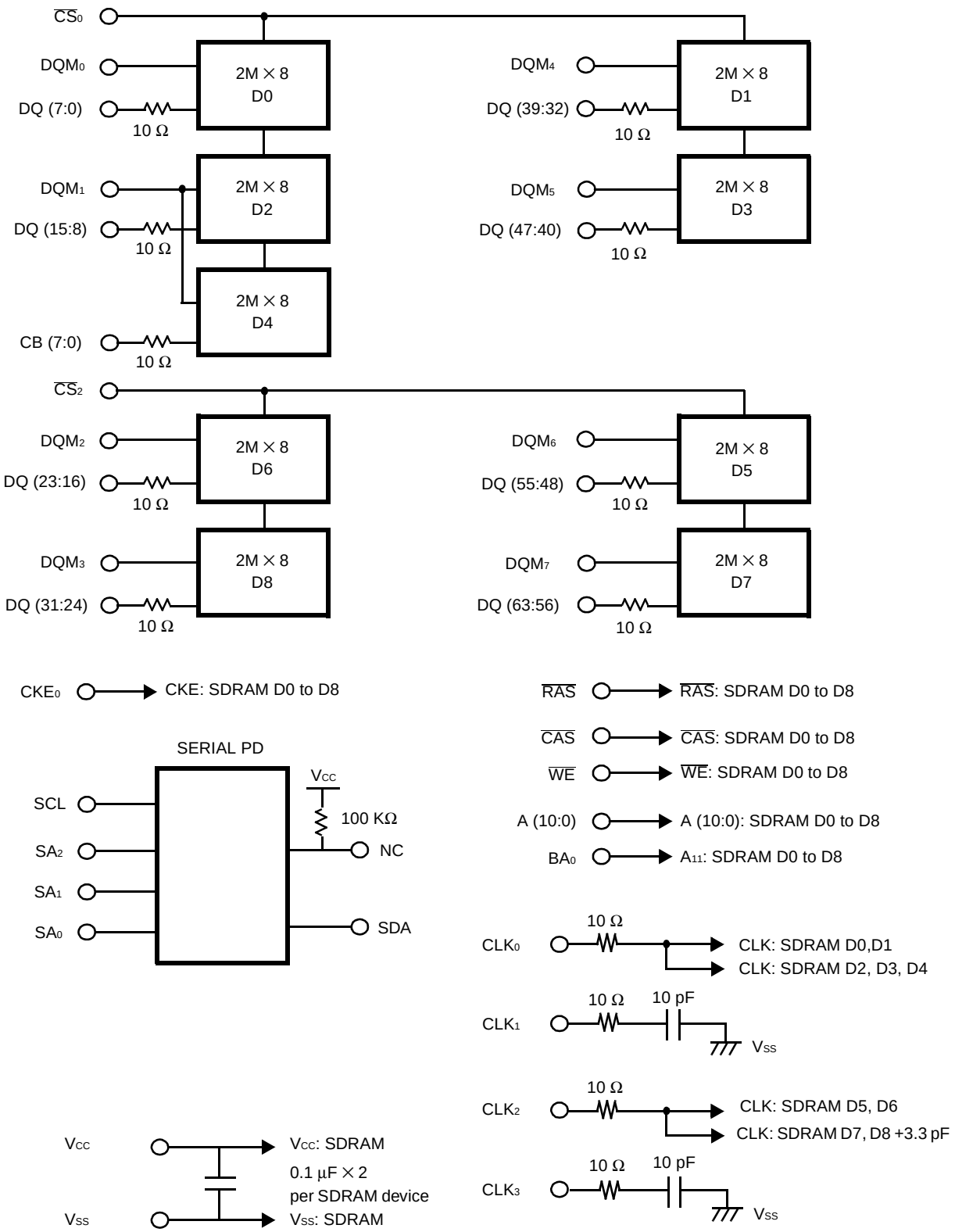
## BLOCK DIAGRAM



## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

| Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| Supply Voltage* | $V_{CC}$ | –0.5 | +4.6 | V |
| Input Voltage* | $V_{IN}$ | –0.5 | +4.6 | V |
| Output Voltage* | $V_{OUT}$ | –0.5 | +4.6 | V |
| Storage Temperature | $T_{STG}$ | –55 | +125 | °C |
| Power Dissipation | $P_D$ | — | 11.7 | W |
| Output Current (D.C.) | $I_{OUT}$ | –50 | +50 | mA |

* : Voltages referenced to $V_{SS}$ (= 0 V)

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

| Parameter | Notes | Symbol | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Supply Voltage | | $V_{CC}$ | 3.0 | 3.3 | 3.6 | V |
| | | $V_{SS}$ | 0 | 0 | 0 | V |
| Input High Voltage, All Inputs | *1 | $V_{IH}$ | 2.0 | — | $V_{CC}$ +0.5 | V |
| Input Low Voltage, All Inputs | *2 | $V_{IL}$ | –0.5 | — | 0.8 | V |
| Ambient Temperature | | $T_A$ | 0 | — | +70 | °C |

*1. Overshoot limit : $V_{IH}$ (max.) = TBD

*2. Undershoot limit : $V_{IL}$ (min) = –1.5 V AC (Pulse Width ≤ 5 ns)

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

# MB8502S072BZ-75/-102/-10

## ■ CAPACITANCE

($V_{CC}$ = +3.3 V, f = 1 MHz, $T_A$ = +25°C)

| Parameter | | Symbol | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| Input Capacitance | $A_0$ to $A_{10}$, $BA_0$ | $C_{IN1}$ | — | 62 | pF |
| | $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ | $C_{IN2}$ | — | 67 | pF |
| | $\overline{CS}_0$, $\overline{CS}_2$ | $C_{IN3}$ | — | 36 | pF |
| | $CKE_0$ | $C_{IN4}$ | — | 62 | pF |
| | $CLK_0$ to $CLK_3$ | $C_{IN5}$ | — | 45 | pF |
| | $DQMB_0$ to $DQMB_7$ | $C_{IN6}$ | — | 21 | pF |
| | SCL | $C_{SCL}$ | — | 6 | pF |
| | $SA_0$, $SA_1$, $SA_2$ | $C_{SA}$ | — | 6 | pF |
| Input/Output Capacitance | SDA | $C_{SDA}$ | — | 6 | pF |
| | $DQ_0$ to $DQ_{63}$ | $C_{DQ}$ | — | 13 | pF |
| | $CB_0$ to $CB_7$ | $C_{CB}$ | — | 13 | pF |

## ■ DC CHARACTERISTICS

**(At recommended operating conditions unless otherwise noted.)**

| Parameter | Notes | | Symbol | Condition | Value | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | |
| Operating Current (Average Power Supply Current) | *1 | MB8502S072BZ-75 | $I_{CC1S}$ | Burst Length = 4, $t_{RC}$ = min for BL = 4, $t_{CK}$ = min, One Bank Active, Outputs Open, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 900 | mA |
| | | MB8502S072BZ-102 | | | | 900 | mA |
| | | MB8502S072BZ-10 | | | | 720 | mA |
| | | MB8502S072BZ-75 | $I_{CC1D}$ | Burst Length = 4, $t_{RC}$ = min for BL = 4, $t_{CK}$ = min, All Banks Active, Outputs Open, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 1350 | mA |
| | | MB8502S072BZ-102 | | | | 1260 | mA |
| | | MB8502S072BZ-10 | | | | 1080 | mA |
| Precharge Standby Current (Power Supply Current) | | | $I_{CC2P}$ | CKE = $V_{IL}$, $t_{CK}$ = min, All Banks Idle, Power Down Mode, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 3.6 | mA |
| | | | $I_{CC2PS}$ | CKE = $V_{IL}$, CLK = $V_{IH}$ or $V_{IL}$, All Banks Idle, Power Down Mode, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 3.6 | mA |
| | *1 | MB8502S072BZ-75 | $I_{CC2N}$ | CKE = $V_{IH}$, $t_{CK}$ = min, All Banks Idle, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 243 | mA |
| | | MB8502S072BZ-102 | | | | 180 | |
| | | MB8502S072BZ-10 | | | | 180 | |
| | | | $I_{CC2NS}$ | CKE = $V_{IH}$, CLK = $V_{IH}$ or $V_{IL}$, All Banks Idle, Input Signal are Stable, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 135 | mA |
| Active Standby Current (Power Supply Current) | | | $I_{CC3P}$ | CKE = $V_{IL}$, $t_{CK}$ = min, Any Bank Active, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 45 | mA |
| | | | $I_{CC3PS}$ | CKE = $V_{IL}$, CLK = $V_{IH}$ or $V_{IL}$, Any Bank Active, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 27 | mA |
| | *1 | MB8502S072BZ-75 | $I_{CC3N}$ | CKE = $V_{IH}$, $t_{CK}$ = min, Any Bank Active, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 486 | mA |
| | | MB8502S072BZ-102 | | | | 360 | |
| | | MB8502S072BZ-10 | | | | 360 | |
| | | | $I_{CC3NS}$ | CKE = $V_{IH}$, CLK = $V_{IH}$ or $V_{IL}$, Any Bank Active, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 225 | mA |

*(Continued)*

# MB8502S072BZ-75/-102/-10

*(Continued)*

| Parameter | Notes | | Symbol | Condition | Value | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | |
| Burst Mode Current (Average Power Supply Current) | *1 | MB8502S072BZ-75 | $I_{CC4}$ | $t_{CK}$ = min, Gapless data, Burst Length = 4, Outputs open, Multiple-banks Active, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 1350 | mA |
| | | MB8502S072BZ-102 | | | — | 1080 | mA |
| | | MB8502S072BZ-10 | | | — | 1080 | mA |
| Auto-refresh Current (Average Power Supply Current) | *1 | MB8502S072BZ-75 | $I_{CC5}$ | Auto Refresh, $t_{CK}$ = min, $t_{RC}$ = min, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 900 | mA |
| | | MB8502S072BZ-102 | | | — | 720 | mA |
| | | MB8502S072BZ-10 | | | — | 720 | mA |
| Self-refresh Current (Average Power Supply Current) | | | $I_{CC6}$ | Self-refresh, $t_{CK}$ = min, CKE ≤ 0.2 V, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 3.6 | mA |
| | | | $I_{CC6A}$ | Asynchronous Self-refresh (by CLK stop) CKE ≤ 0.2 V, CLK = $V_{IL}$, 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ | — | 3.6 | mA |
| Input Leakage Current (All Inputs) | | | $I_{LI}$ | 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ All other pins not under test = 0 V 3.0 V ≤ $V_{CC}$ ≤ 3.6 V | –50 | 50 | µA |
| Output Leakage Current | | | $I_{LO}$ | Output is disabled (Hi-Z) 0 V ≤ $V_{IN}$ ≤ $V_{CC}$ 3.0 V ≤ $V_{CC}$ ≤ 3.6 V | –10 | 10 | µA |
| LVTTL Output High Voltage | *2 | | $V_{OH}$ | $I_{OH}$ = –2.0 mA | 2.4 | — | V |
| LVTTL Output Low Voltage | *2 | | $V_{OL}$ | $I_{OL}$ = +2.0 mA | — | 0.4 | V |

**Notes:** *1. $I_{CC}$ depends on the output termination, load conditions, clock cycle rate and signal clock rate. The specified values are obtained with the output open and no termination register.

*2. Voltages referenced to $V_{SS}$ (= 0 V)

*3. An initial pause (DESL on NOP) of 200 µs is required after power-on followed by a minimum of eight Auto-refresh cycles.

*4. DC characteristics is the Serial PD standby state ($V_{IN}$ = GND or $V_{CC}$).

## ■ AC CHARACTERISTICS

### (1) BASE CHARACTERISTICS
**(At recommended operating conditions unless otherwise noted.)**

| No. | Parameter | Notes | | Symbol | MB8502S072BZ-75 | | MB8502S072BZ-102 | | MB8502S072BZ-10 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| 1 | Clock Period | | CL = 3 | $t_{CK3}$ | 7.5 | — | 10 | — | 10 | — | ns |
| | | | CL = 2 | $t_{CK2}$ | 11.5 | — | 10 | — | 15 | — | |
| 2 | Clock High Time | | | $t_{CH}$ | 2.5 | — | 3 | — | 3 | — | ns |
| 3 | Clock Low Time | | | $t_{CL}$ | 2.5 | — | 3 | — | 3 | — | ns |
| 4 | Input Setup Time | | | $t_{SI}$ | 2 | — | 2 | — | 2 | — | ns |
| 5 | Input Hold Time | | | $t_{HI}$ | 1 | — | 1 | — | 1 | — | ns |
| 6 | Output Valid from Clock ($t_{CLK}$ = min) | *1, *2 | CL = 3 | $t_{AC3}$ | — | 6 | — | 6 | — | 6 | ns |
| | | | CL = 2 | $t_{AC2}$ | — | 7 | — | 6 | — | 8 | |
| 7 | Output in Low-Z | | | $t_{LZ}$ | 0 | — | 0 | — | 0 | — | ns |
| 8 | Output in High-Z | *3 | CL = 3 | $t_{HZ3}$ | 2 | 6 | 3 | 6 | 3 | 6 | ns |
| | | | CL = 2 | $t_{HZ2}$ | 3 | 7 | 3 | 6 | 3 | 8 | |
| 9 | Output Hold Time | | CL = 3 | $t_{OH}$ | 2 | — | 3 | — | 3 | — | ns |
| | | | CL = 2 | | 3 | — | 3 | — | 3 | — | |
| 10 | Time between Auto-Refresh Command Interval | | | $t_{REFI}$ | — | 15.6 | — | 15.6 | — | 15.6 | µs |
| 11 | Time between Refresh | | | $t_{REF}$ | — | 65.6 | — | 65.6 | — | 65.6 | ms |
| 12 | CKE Low (or CLK Low) Hold Time for Asynchronous Self-Refresh Entry | | | $t_{ASE}$ | 100 | — | 100 | — | 100 | — | µs |
| 13 | Transition Time | | | $t_T$ | 0.5 | 2 | 0.5 | 2 | 0.5 | 2 | ns |
| 14 | CKE Setup Time for Power Down Exit | | | $t_{CKSP}$ | 3 | — | 3 | — | 3 | — | ns |

# MB8502S072BZ-75/-102/-10

## (2) BASE VALUES FOR CLOCK COUNT/LATENCY

| No. | Parameter | Notes | Symbol | MB8502S072BZ -75 | | MB8502S072BZ -102 | | MB8502S072BZ -10 | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| 1 | $\overline{RAS}$ Cycle Time | *4 | $t_{RC}$ | 67.5 | — | 70 | — | 80 | — | ns |
| 2 | $\overline{RAS}$ Precharge Time | | $t_{RP}$ | 22.5 | — | 20 | — | 30 | — | ns |
| 3 | $\overline{RAS}$ Active Time | | $t_{RAS}$ | 45 | 100000 | 50 | 100000 | 50 | 100000 | ns |
| 4 | $\overline{RAS}$ to $\overline{CAS}$ Delay Time | *5 | $t_{RCD}$ | 22.5 | — | 20 | — | 30 | — | ns |
| 5 | Write Recovery Time | | $t_{WR}$ | 7.5 | — | 10 | — | 10 | — | ns |
| 6 | Data-in to Precharge Lead Time | | $t_{DPL}$ | 7.5 | — | 10 | — | 10 | — | ns |
| 7 | Data-in to Active/Refresh Command Period | CL = 3 | $t_{DAL3}$ | 2 cyc + $t_{RP}$ | — | 2 cyc + $t_{RP}$ | — | 2 cyc + $t_{RP}$ | — | ns |
| | | CL = 2 | $t_{DAL2}$ | 1 cyc + $t_{RP}$ | — | 1 cyc + $t_{RP}$ | — | 1 cyc + $t_{RP}$ | — | ns |
| 8 | Mode Register Set Cycle Time | | $t_{RSC}$ | 15 | — | 20 | — | 20 | — | ns |
| 9 | $\overline{RAS}$ to $\overline{RAS}$ Bank Active Delay Time | | $t_{RRD}$ | 15 | — | 20 | — | 20 | — | ns |

## (3) CLOCK COUNT FORMULA (*6)

$$\text{Clock} \geq \frac{\text{Base Value}}{\text{Clock Period}} \quad \text{(Round off a whole number)}$$

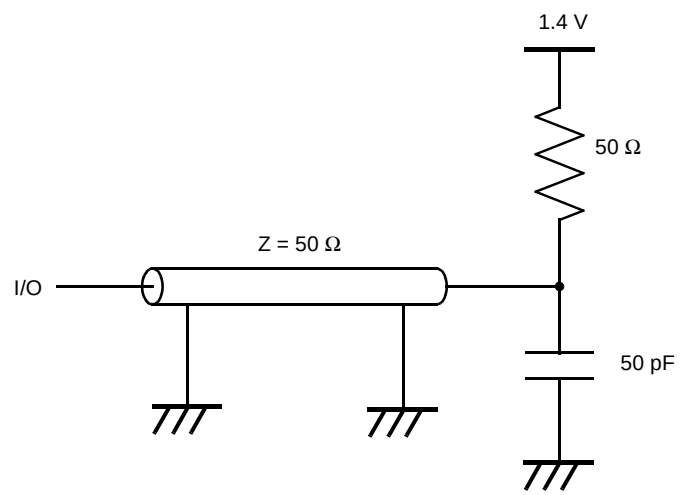
## (4) LATENCY (The latency values on these parameters are fixed regardless of clock period.)

| No. | Parameter | | Symbol | MB8502S072BZ -75 | MB8502S072BZ -102 | MB8502S072BZ -10 | Unit |
|---|---|---|---|---|---|---|---|
| 1 | CKE to Clock Disable | | $I_{CKE}$ | 1 | 1 | 1 | Cycle |
| 2 | DQM to Output in High-Z | | $I_{DQZ}$ | 2 | 2 | 2 | Cycle |
| 3 | DQM to Input Data Delay | | $I_{DQD}$ | 0 | 0 | 0 | Cycle |
| 4 | Last Output to Write Command Delay | | $I_{OWD}$ | 2 | 2 | 2 | Cycle |
| 5 | Write Command to Input Data Delay | | $I_{DWD}$ | 0 | 0 | 0 | Cycle |
| 6 | Precharge to Output in High-Z Delay | CL = 3 | $I_{ROH3}$ | 3 | 3 | 3 | Cycle |
| | | CL = 2 | $I_{ROH2}$ | 2 | 2 | 2 | Cycle |
| 7 | Burst Stop Command to Output in High-Z Delay | CL = 3 | $I_{BSH3}$ | 3 | 3 | 3 | Cycle |
| | | CL = 2 | $I_{BSH2}$ | 2 | 2 | 2 | Cycle |
| 8 | $\overline{CAS}$ to $\overline{CAS}$ Delay (min) | | $I_{CCD}$ | 1 | 1 | 1 | Cycle |
| 9 | $\overline{CAS}$ Bank Delay (min) | | $I_{CBD}$ | 1 | 1 | 1 | Cycle |

**Notes:** *1. Assumes $t_{RCD}$ is satisfied.
*2. $t_{AC}$ also specifies the access time at burst mode except for first access.
*3. Specified where output buffer is no longer driven.
*4. Actual clock count of $t_{RC}$ ($I_{RC}$) will be sum of clock count of $t_{RAS}$ ($I_{RAS}$) and $t_{RP}$ ($I_{RP}$).
*5. Operation within the $t_{RCD}$ (min) ensures that access time is determined by $t_{RCD}$ (min) + $t_{AC}$ (max); if $t_{RCD}$ is greater than the specified $t_{RCD}$ (min), access time is determined by $t_{AC}$.
*6. All base values are measured from the clock edge at the command input to the clock edge for the next command input.
All clock counts are calculated by a simple formula:
clock count equals base value divided by clock period (round off to a whole number).
*7. An initial pause (DESL on NOP) of 200 µs is required after power-up followed by a minimum of eight Auto-refresh cycles.
*8. 1.4 V or $V_{REF}$ is the reference level for measuring timing of signals.
Transition times are measured between $V_{IH}$ (min) and $V_{IL}$ (max).
*9. AC characteristics assume $t_T$ = 1 ns and 50 pF of capacitive load.

*Source: See MB81F16822B Data Sheet for details on the electricals.

## ■ AC OPERATING TEST CONDITION (Example of AC Test Load Circuit)



# MB8502S072BZ-75/-102/-10

## ■ SERIAL PRESENCE DETECT(SPD) FUNCTION

### 1. PIN DESCRIPTIONS

**SCL (Serial Clock)**

SCL input is used to clock all data input/output of SPD

**SDA (Serial Data)**

SDA is a common pin used for all data input/output of SPD. The SDA pull-up resistor is required due to the open-drain output.

**$SA_0$, $SA_1$, $SA_2$ (Address)**

Address inputs are used to set the least significant three bits of the eight bits slave address. The address inputs must be fixed to select a particular module and the fixed address of each module must be different each other.

### 2. SPD OPERATIONS

**CLOCK and DATA CONVENTION**

Data states on the SDA can change only during SCL = Low. SDA state changes during SCL = High are indicated start and stop conditions. Refer to Fig. 1 below.

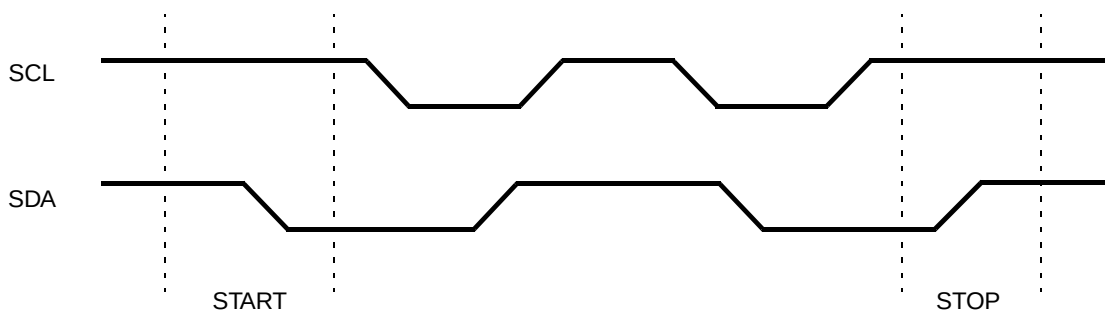
**START CONDITION**

All commands are preceded by a start condition, which is a transition of SDA state from High to Low when SCL = High. SPD will not respond to any command until this condition has been met.

**STOP CONDITION**

All read or write operation must be terminated by a stop condition, which is a transition of SDA state from Low to High when SCL = High. The stop condition is also used to make the SPD into the state of standby power mode after a read sequence.

**Fig. 1 – START AND STOP CONDITIONS**




START = High to Low transition of SDA state when SCL is High

STOP = Low to High transition of SDA state when SCL is High

**ACKNOWLEDGE**

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will put the SDA line to Low in order to acknowledge that it received the eight bits of data.

The SPD will respond with an acknowledge when it received the start condition followed by slave address issued by master.

In the read operation, the SPD will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is issued by master, the SPD will continue to transmit data. If an acknowledge is not detected, the SPD will terminated further data transmissions. The master must then issue a stop condition to return the SPD to the standby power mode.

In the write operation, upon receipt of eight bits of data the SPD will respond with an acknowledge, and await the next eight bits of data, again responding with an acknowledge until the stop condition is issued by master.

**SLAVE ADDRESS ADDRESSING**

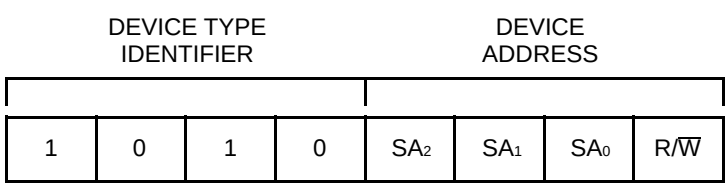
Following a start condition, the master must output the eight bits slave address. The most significant four bits of the slave address are device type identifier. For the SPD this is fixed as 1010[B]. Refer to the Fig. 2 below.

The next three significant bits are used to select a particular device. A system could have up to eight SPD devices —namely up to eight modules— on the bus. The eight addresses for eight SPD devices are defined by the state of the $SA_0$, $SA_1$ and $SA_2$ inputs.

The last bit of the slave address defines the operation to be performed. When R/$\overline{W}$ bit is “1”, a read operation is selected, when R/$\overline{W}$ bit is “0”, a write operation is selected.

Following the start condition, the SPD monitors the SDA line comparing the slave address being transmitted with its slave address (device type and state of $SA_0$, $SA_1$, and $SA_2$ inputs). Upon a correct compare the SPD outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the SPD will execute a read or write operation.

**Fig. 2 – SLAVE ADDRESS**

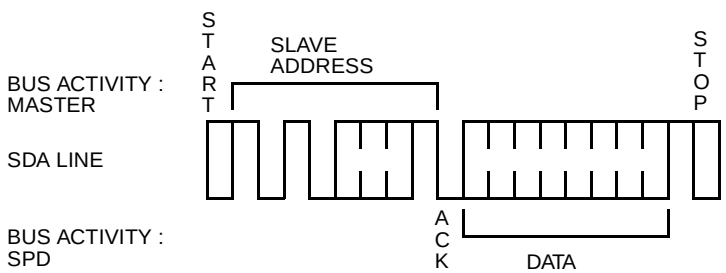


## 3. READ OPERATIONS

### CURRENT ADDRESS READ

Internally the SPD contains an address counter that maintains the address of the last data accessed, incremented by one. Therefore, if the last access (either a read or write operation) was to address(n), the next read operation would access data from address(n+1). Upon receipt of the slave address with the R/$\overline{W}$ bit = “1”, the SPD issues an acknowledge and transmits the eight bits of data during the next eight clock cycles. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig. 3 for the sequence of address, acknowledge and data transfer.

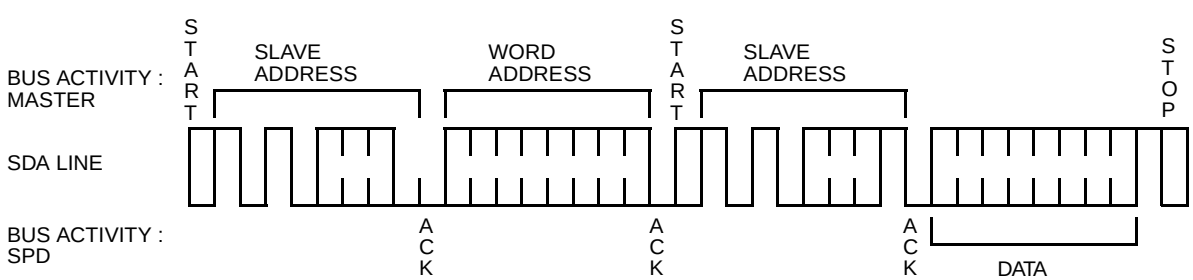
**Fig. 3 – CURRENT ADDRESS READ**




### RANDOM READ

Random Read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit = “1”, the master must first perform a “dummy” write operation on the SPD. The master issues the start condition, and the slave address followed by the word address. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit = “1”. This will be followed by an acknowledge from the SPD and then by the eight bits of data. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig. 4 for the sequence of address, acknowledge and data transfer.

**Fig. 4 – RANDOM READ**

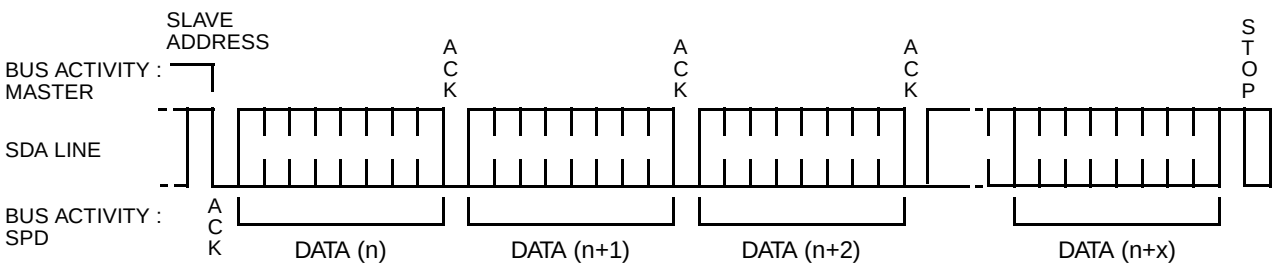


### SEQUENTIAL READ

Sequential Read can be initiated as either a current address read or random read. The first data are transmitted as with the other read mode, however, the master now responds with an acknowledge, indicating it requires additional data. The SPD continues to output data for each acknowledge received. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig. 5 for the sequence of address, acknowledge and data transfer.

The data output is sequential, with the data from address(n) followed by the data from address(n+1). The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255), the counter “rolls over” to address 0 and the SPD continues to output data for each acknowledge received.

**Fig. 5 – SEQUENTIAL READ**




## 4. DC CHARACTERISTICS

| Parameter | Note | Symbol | Condition | Value | | Unit |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Input Leakage Current | | $S_{ILI}$ | $0\ V \le V_{IN} \le V_{CC}$ | –10 | 10 | µA |
| Output Leakage Current | | $S_{ILO}$ | $0\ V \le V_{OUT} \le V_{CC}$ | –10 | 10 | µA |
| Output Low Voltage | *1 | $S_{VOL}$ | $I_{OL}$ = 3.0 mA | — | 0.4 | V |

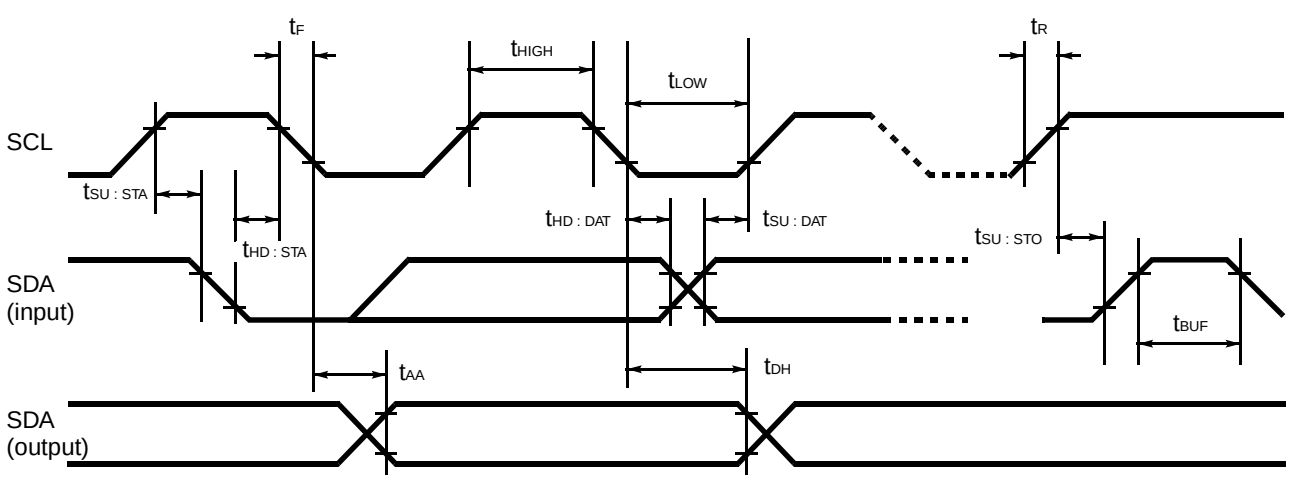
**Note:** *1. Referenced to $V_{SS}$.

# MB8502S072BZ-75/-102/-10

## 5. AC CHARACTERISTICS

| No. | Parameter | Symbol | Value | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| 1 | SCL Clock Frequency | $f_{SCL}$ | — | 100 | KHz |
| 2 | Noise Suppression Time Constant at SCL, SDA Inputs | $T_I$ | — | 100 | ns |
| 3 | SCL Low to SDA Data Out Valid | $t_{AA}$ | — | 3.5 | µs |
| 4 | Time the Bus Must Be Free Before a New Transmission Can Start | $t_{BUF}$ | 4.7 | — | µs |
| 5 | Start Condition Hold Time | $t_{HD:STA}$ | 4.0 | — | µs |
| 6 | Clock Low Period | $t_{LOW}$ | 4.7 | — | µs |
| 7 | Clock High Period | $t_{HIGH}$ | 4.0 | — | µs |
| 8 | Start Condition Setup Time | $t_{SU:STA}$ | 4.7 | — | µs |
| 9 | Data in Hold Time | $t_{HD:DAT}$ | 0 | — | µs |
| 10 | Data in Setup Time | $t_{SU:DAT}$ | 250 | — | ns |
| 11 | SDA and SCL Rise Time | $t_R$ | — | 1 | µs |
| 12 | SDA and SCL Fall Time | $t_F$ | — | 300 | ns |
| 13 | Stop Condition Setup Time | $t_{SU:STO}$ | 4.7 | — | µs |
| 14 | Data Out Hold Time | $t_{DH}$ | 100 | — | ns |
| 15 | Write Cycle Time | $t_{WR}$ | — | 15 | ms |

**Fig. 6 – TIMING WAVEFORM**



## ■ PACKAGE DIMENSION

168-pin plastic DIMM (socket type)
(MDS-168P-P25)

**T.B.D.**

Dimension in mm (inches)

# MB8502S072BZ-75/-102/-10

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